THE TIME KEEPING SYSTEM FOR GPS BLOCK IIR

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Abstract

The precision time keeping system (TKS) in the Global Positioning System (GPS), Block IIR satellites is designed to operate under severe natural and man made environmental conditions. The Block IIR TKS provides precise, autonomous time keeping for periods of up to seven months, without the intervention of the GPS Control Segment. The TKS is implemented using both linear and non–linear controls. The resulting TKS architecture uses a hybrid analog/digital phase locked loop (PLL). The paper provides details of the design and analysis of the TKS. The simulation techniques and the test bed activities used in performing the TKS design trade–offs are described. The effects of non–linear controls are analyzed using a TKS computer simulation of the PLL. The results from a hardware test bed are provided that verify desired TKS operation. The design criteria for the TKS computer simulation and the hardware test bed are indicated. The concepts for verification and testing of the TKS computer simulation and hardware test bed are presented.

GPS BLOCK IIR

Global Positioning System (GPS) is an all weather, worldwide, passive navigation system that is currently in use for a variety of land, water, air, and space navigation applications. ITT Aerospace/Communications Division(ITT A/CD) is a leader in the development of space payloads and has been involved in the design of various portions of the GPS space segment from the inception in mid '70s. ITT is currently developing the Total Navigation Payload (TNP) for the next generation (Block IIR) GPS satellites. Block IIR GPS satellites provide longer life, improved performance, crosslink ranging and enhanced crosslink communication capabilities. The Block IIR TNP also provides autonomous operation for up to 210 days without Control Segment intervention. Autonomous navigation is achieved using a two way ranging and data exchange process between the GPS satellites in the constellation. Further details of GPS Block IIR Autonomous Navigation (AutoNav) can be found in [1].

TIME KEEPING SYSTEM

The Time Keeping System (TKS) is the heart of the GPS TNP and provides an accurate time base for each satellite in the GPS system. TKS derived timings are used to provide accurate timing for

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the other payloads in the GPS satellites and also constitutes the reference to the navigation ranging signals. GPS user receivers determine accurate time, 3D position and 3D velocity by measuring ranges and range rates to a set of four GPS satellites. The accuracy of the user's position, velocity and time determination depends on the accuracy of the data transmitted to the user, the geometry of the four satellites used and the precision of the TKS system.

TKS ARCHITECTURE

The TKS loop architecture is a Phase Lock Loop (PLL) based implementation that has enhanced single event upset and radiation performance. Figure 1 shows the block diagram of the TKS architecture. A detailed description of the TKS architecture can be found in [2]. The TKS system utilizes two frequency sources, one is a reference frequency source (derived from an atomic frequency standard) and the other is a system frequency source (derived from a VCXO). The system frequency source (10.23 MHz) is the output of the TKS system that provides precise timing to GPS satellites. The two frequency sources are coupled via a sampled data control loop, referred to as the TKS PLL. The 10.23 MHz TKS system clock has the excellent short term stability of the VCXO and the excellent long term stability of the atomic frequency standard (AFS). The exact value of the AFS's natural frequency is not critical. The TKS system can be used with either a Cesium AFS (CAFS) or a Rubidium AFS (RAFS). This paper will primarily concentrate on TKS performance when using RAFS. The AFSs natural frequency is approximately 13.4 MHz. The two frequency sources are independently divided to provide a 1.5 second reference epoch signal and a 1.5 second system epoch signal. The phase difference between these two signals are precisely measured by a hardware phase meter. The output of the phase meter is the driving signal for the TKS PLL which is implemented in software.

TKS LOOP

The TKS phase lock loop (PLL) combines: (1) the excellent short term stability of a voltage controlled crystal oscillator (VCXO) to enable superior short time interval TKS accuracy, and (2) the excellent long term stability of the AFS to enable superior long time interval TKS accuracy. The selection of the loop time constant enables proper selection of this crossover between VCXO and AFS stabilities. Varying the crossover time interval will have an impact on the TKS output Allan Variance. A shorter crossover interval increases the contribution of hardware component noise to the Allan variance. A longer crossover interval increases the contribution of VCXO drift to the Allan variance. Effects of this trade–off are discussed later using simulation results.

The software implementation of the control loop also allows clock corruptions to be easily added to limit the accuracy provided to unauthorized GPS users. To maintain full accuracy for the authorized users who have access to the clock corruptions, the gain of the VCXO has to be periodically estimated. The TKS performs an open loop gain characterization of the VCXO initially, and subsequently, when the loop is closed and tracking, the gain is periodically updated using a minimum mean square estimator. The estimated gain of the VCXO from its digital frequency command to its analog frequency output (the VCXO transfer function) is compensated for by the gain control so that the gain from the output of the PLL compensation filter to the VCXO output is kept at unity to within small fractions of a percent under all conditions. This compensation enables the

authorized users to achieve the full accuracy of the TKS system. Without the compensation, this gain could vary several percent causing noticeable TKS accuracy degradation.

The heart of the gain control is an equation which has as its input the digital frequency command from the PLL loop filter and as its output the digital control value that drives the VCXO input. The gain tracking uses a localized linear equation around the operating point of the VCXO. The gain control technique takes advantage of the small variations used for clock corruptions, as they are within the linear range of the VCXO at normal operating points. The gain tracking algorithm measures the changes in the VCXO transfer function during the period the clock corruptions are being applied. Any changes in gain are decoupled from the PLL output by modifying the frequency command at the same time the gain equation is changed so that the output will not exhibit any step changes. The performance improvements achieved using gain compensation are described in later sections.

TKS SIMULATION

The TKS simulation activity was undertaken: (1) to get insight into the performance prior to the availability of flight hardware and software, (2) to evaluate the algorithms for compliance to required performance, (3) to refine the algorithms and simplify them for ease of implementation, (4) to perform algorithm trade–offs and (5) to reduce development risk. The simulation also allowed the algorithms to be verified at an accelerated time compared to real-time, and used a higher order programming language, enabling faster performance evaluation.

The TKS simulation implements the difference equations that describe the Z transform of the TKS hardware, and the algorithms of the TKS software. The hardware error sources are also modeled. The block diagram of the TKS simulation is shown in Figure 2.

There are three major error sources in the TKS system, namely: the AFS, the VCXO, and the phase meter. The phase meter outputs the digital phase difference between the two oscillators and is the error detector for the PLL. In order to accurately simulate the PLL, the three error sources are modeled by noise generators that have the specified Allan Variance of each error source.

The AFS noise is simulated by combining two Allan Variance noise generators, an initial slope of $\tau^{-0.5}$ for small and moderate τ, and a final slope of τ^{0} for large TAU. The actual AFS has a slope of τ^{0} for very small τ. This can be ignored because the PLL bandwidth is such that the PLL dramatically attenuates the Allan Variance of the AFS input for TAUs almost an order of magnitude larger than the maximum τ of the ignored portion. The inherent drift of the AFS is also ignored because the GPS Control Segment measures and compensates for that drift as part of its normal procedures. The resulting Allan Variance of the RAFS is shown in Figure 3.

The phase meter noise is simulated using a uniform random number generator. The TKS phase meter has a 600 MHz oscillator which is used to measure the length of the phase interval. The random number represents the phase of the oscillator at the start of the phase error interval. The output of the simulated phase meter is the oscillator period multiplied by the number of counts in the phase error interval. The phase meter noise is the difference between the phase meter output and the actual phase error interval. Drift in the frequency of the phase meter oscillator can be neglected as it causes an insignificant change in the quantization interval. Random noise pickup

in the phase meter circuitry is also neglected due to its high frequency nature compared to the forward path bandwidth of the PLL. The resulting Allan Variance of the phase meter is shown in Figure 4.

The VCXO noise is simulated using an Allan Variance noise generator with an initial slope of τ^0 for small τs and an Allan Variance noise generator with a slope of $\tau^{0.5}$ for moderate and large TAUs to represent the drift in the VCXO. The resulting Allan Variance of the VCXO is shown in Figure 5.

The Allan Variance noise generator used for generating a τ^0 slope is a modified version of the one presented in [3]. The Allan Variance noise generator used for generating a $\tau^{-0.5}$ slope is obtained by integrating the output of a Gaussian random number generator. The Allan Variance noise generator used for generating a $\tau^{0.5}$ slope is obtained by double integrating the output of a Gaussian random number generator.

TKS HARDWARE TEST BED

The TKS hardware test bed, which consists of brassboard and engineering development model (EDM) hardware, was used to accelerate development of TKS algorithms on the real hardware, prior to the availability of flight hardware. The test bed provided an early, fast, low cost demonstration of the feasibility of the VCXO loop and validated the performance of the operational hardware, and the TKS algorithms. The test bed also provided confirmation of the correctness of the TKS simulation model. The use of off the shelf hardware and test software with only the functions needed to test the PLL has made the cost of the hardware test bed minimal. The test bed activities enabled improvements in hardware and software. The test bed was upgraded as more and more flight like hardware were available. The test bed activities provided considerable reduction in the development risk of the flight hardware meeting TKS performance needs. It also enabled a through testing of the TKS with specially designed test bed tests. The following paragraphs describe the test bed development.

The initial test bed had no EDM hardware. The AFS 13.4 Mhz signal was provided by a HP 3325B synthesizer driven by an off the shelf EG&G 10 MHz RFS-10 Rubidium oscillator. The reference and system epoch generators used existing counters which ITT A/CD had built as part of a demonstration unit for a precursor program to the present GPS Block IIR program. The software algorithms were programmed and executed using the C language on an IBM compatible AT 286 PC. The phase meter function was performed by an off the shelf GT–100 Universal Counter PC card with a precision of 0.1 nanoseconds. The test bed used a demonstration unit digital VCXO at 10.23 MHz (nominal center frequency) with a digital input that drove two precision digital to analog converters to control the output frequency.

The initial test bed demonstrated the feasibility of generating a precision GPS 10.23 MHz signal using a VCXO that was locked to an AFS at a different non harmonically related frequency. The output signal was phase locked to the AFS, with and without clock corruptions, to within a fraction of a nanosecond. This initial demonstration program used externally generated values for centering the VCXO and compensating for the VCXO transfer function.

In the past year, as EDM hardware became available, they were incorporated into the test bed and

checked out. First, the demonstration VCXO was replaced by a single thread VCXO with the same input controls as the EDM unit and then the single thread unit was replaced by a dual unit flight configuration EDM VCXO. Also a phase meter which has the same 600 MHz counting technique and the same 1.67 nanosecond quantizing noise as the flight phase meter was incorporated into the test bed. In addition, the software was upgraded to use the operational centering, VCXO gain control and gain tracking. The rest of the hardware was unchanged except that the PC was upgraded to a 386 machine. With the new software and hardware, the test bed TKS system could center, characterize, and track the AFS to a fraction of a nanosecond without any outside values or assistance.

The test bed performance was compared to the prediction of the TKS simulator and theoretical calculations. As shown below, there was agreement between the measured test bed performance and the predicted performance. The success of the cross check has provided confidence in the GPS TKS design in general, including the correctness of the hardware design, the software algorithms, and the TKS simulator.

CO–VERIFICATION OF TKS SIMULATION AND TEST BED

The first step to co–verification was to insert a step function into the error in the PLL hardware test bed. This was accomplished by adding a constant to the digitized error in the test bed control computer and monitoring the digitized error after the step function insertion point for a period of time. Exactly the same step function was inserted at exactly the same point in the simulation and exactly the same monitoring was performed. Figure 6 shows an overlay of the two monitored points, one in the simulation and one in the test bed. Note that the two transients differed only by the noise pickup present at the test bed error point. This showed that the deterministic dynamics of the test bed and the simulation matched.

The next step was to record the digitized steady state error at the output of the phase meter of the hardware test bed and exactly the same point in the simulation. These errors were then used to compute the Allan Variance of the phase meter error for the hardware test bed and the simulation. The shape of the Allan Variance curves matched, however the amplitude was different. The difference was due to the smaller quantization of the purchased phased meter initially used in the test bed.

A brassboard phase meter was built which used the same design parameters as the production phase meter. This unit was placed in the test bed. There was initially a question as to whether the brassboard unit was working as designed. Open loop tests of the phase meter were performed, but inherent drifts in the test bed prevented statistically usable results. The solution was to sample the closed loop, steady state error at the output of the phase meter in the test bed and compute its Allan Variance for comparison to the equivalent Allan Variance from the simulation. Figure 7 shows the results with the PLL subject to pseudo clock corruptions and on line gain tracking. Note that at low TAU where the phase meter noise would dominate, there was less than 10% difference between the Allan Variance curves from the test bed and the simulation. This led us to the conclusion that the simulation of the phase meter was correct, that the brassboard phase meter was also operating as designed, and that the difference was attributable to the noise pickup in the system.

TKS PERFORMANCE TRADE–OFFS

The bandwidth of the PLL is chosen to achieve the best TKS Allan Variance (at the output of the PLL). This selected bandwidth is such that it attenuates the effects of the AFS and the phase meter for small TAU and the effect of the VCXO for large TAU. Figure 8 shows that if the PLL time constant is too small, the phase meter noise at the output get too large. It also shows that if the PLL loop time constant is too long, the drift of the VCXO gets too large. The result was a loop time constant which was a tradeoff between the two noise effects at the output of the PLL.

The bandwidth of the PLL also affects the transient responses to steps and ramps that might be caused by an undesired severe environmental disturbance. Figure 9 shows how the transient response changes as a function of the PLL time constant. It shows that the smaller the time constant, the faster the response and the smaller the peak. Therefore the smaller time constant is desirable from a transient point of view. The TKS design uses a dual time constant: a short time constant during transients and a long time constant during steady state. Figure 10 compares the initial lock–on transient using switched, dual time constants and using a single long time constant. The reduction in settling time and amplitude deviation is dramatic.

The PLL has to operate closed loop to make the VCXO output exactly follow the AFS phase plus the clock corruptions that have been introduced. The simulation was used to determine the effect of clock corruptions on the closed loop operation compared to a case with no corruption. Clearly the unauthorized users who do not have access to the clock corruptions will see their time, range, and range rate accuracies degrade. On the other hand, the authorized users who have access to the clock corruption values can remove the effects of the clock corruptions and achieve full accuracy of the TKS. Figure 11 shows that there is a very small increase in the Allan Variance at the output of the PLL when clock corruptions are in effect. This will be the TKS performance available to the authorized users.

The implementation of clock corruptions as an open loop perturbation requires VCXO gain tracking. The algorithm for gain tracking was implemented in both the simulation and the test bed. Figure 12 shows the computer simulation output Allan Variance with and without gain tracking. There was no significant difference between the two graphs. Note that Figure 7 is the Allan Variance for the test bed and the computer simulation of the phase meter output in the presence of clock corruptions and gain tracking. The results agree to within about 10-20%. This shows that the hardware and the simulation agree, validating the VCXO characterization and gain tracking approaches and algorithms in the presence of clock corruptions.

To insure that there was no interaction between the stability of the system and the non-linear characteristics of the VCXO gain tracking algorithms, a BODE plot was made of the simulation with gain tracking activated. Figure 13 is the results of this test and indicate that there is no detectable deviation in the BODE plot with and without gain tracking. Also, the BODE plot is what was expected based on the deterministic design of the PLL, and shows sufficient gain and phase margins, ensuring the stability of the design.

CONCLUSIONS

As expected, the simulation and test bed activities were valuable tools that enabled the TKS design and development, prior to the availability of the flight hardware, thereby mitigating the development risk. The resulting TKS design with dual time constant has excellent transient behavior and steady state stability, providing a near optimal TKS system.

ACKNOWLEDGEMENTS

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[2] Baker, A., *"GPS Block IIR Time Standard Assembly Architecture."*, presented at the 22nd Annual PTTI Meeting in Dec. '90, pp. 317–324.

[3] Barnes, J. A., and Greenhall, C. A., *"Large Sample Simulation Of Flicker Noise"*, presented at the 19th Annual PTTI Meeting in Dec. '87, pp. 203–217.

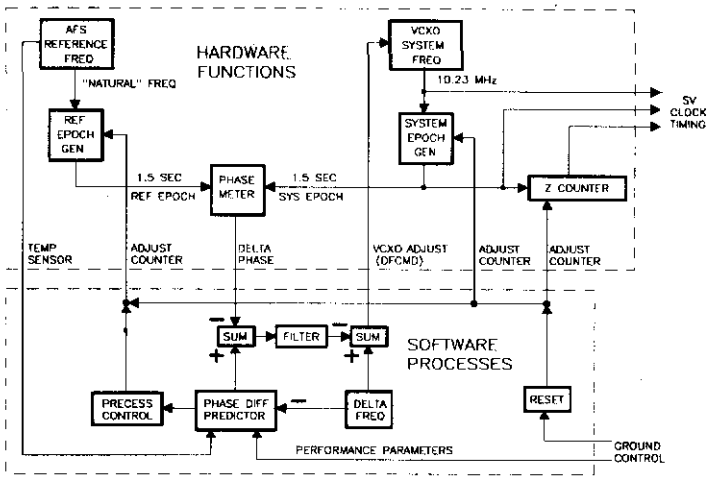


Figure 1: TKS Architecture

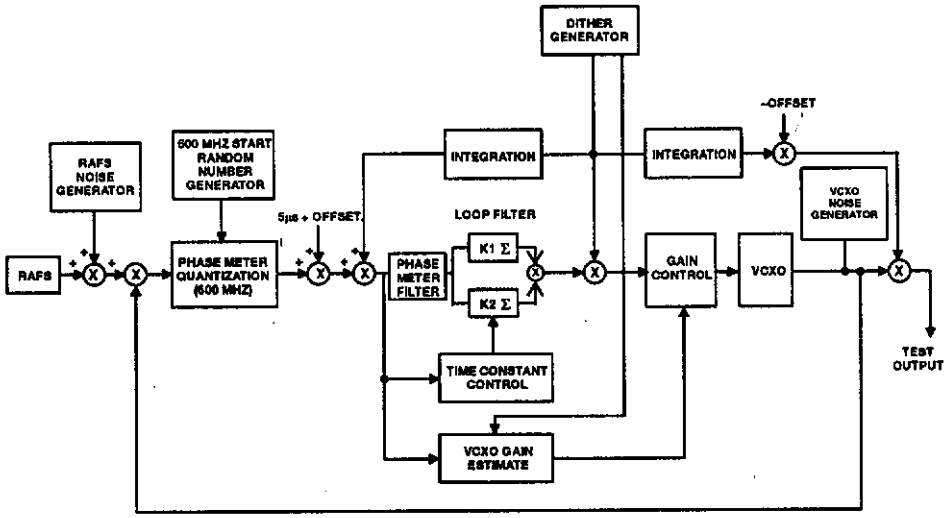


Figure 2: TKS Simulation Signal Flow

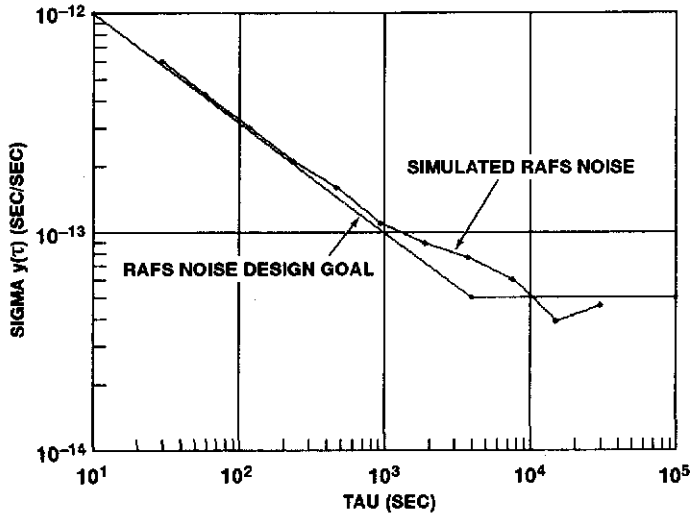


Figure 3: Simulated RAFS Allan Variance

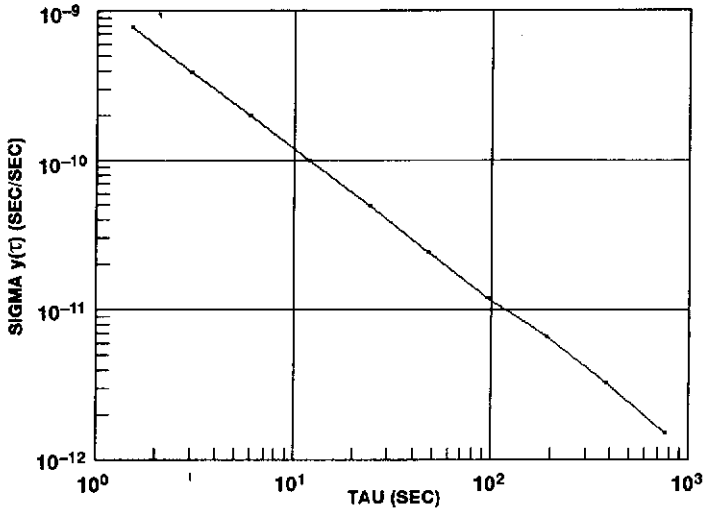


Figure 4: Simulated Phase Meter Allan Variance

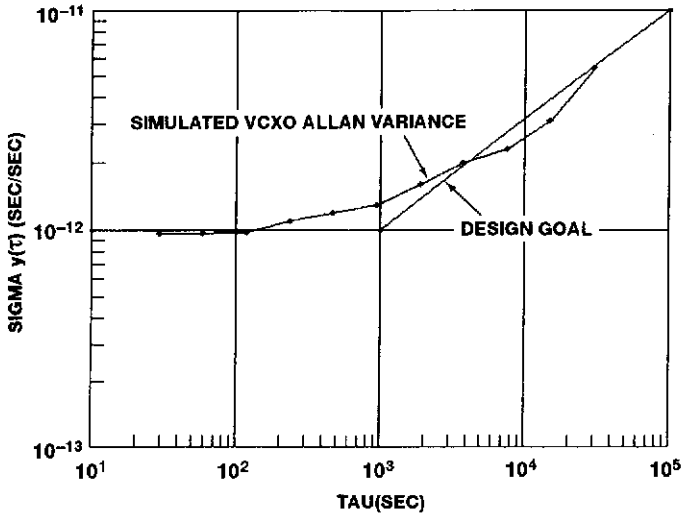


Figure 5: Simulated VCXO Allan Variance

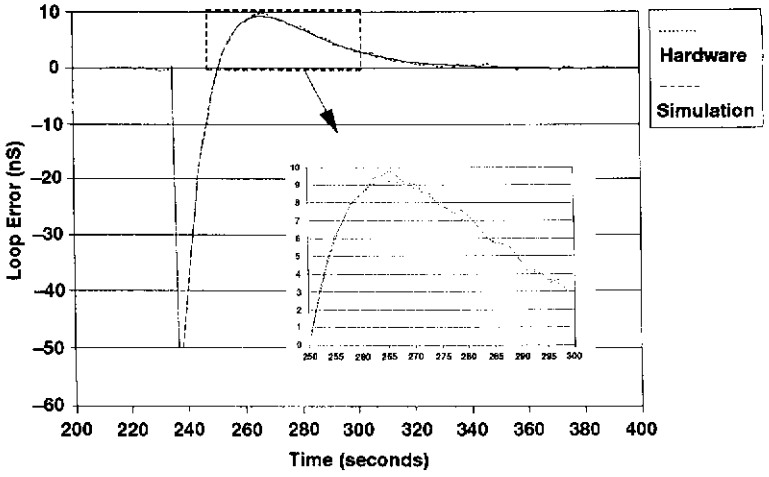


Figure 6: Phase Jump Response of TKS Test Bed and Simulation

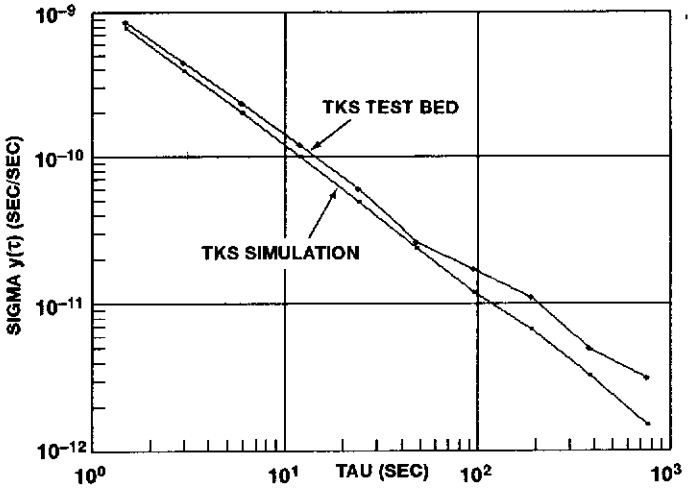


Figure 7: Loop Error Allan Variance of TKS Test Bed and Simulation

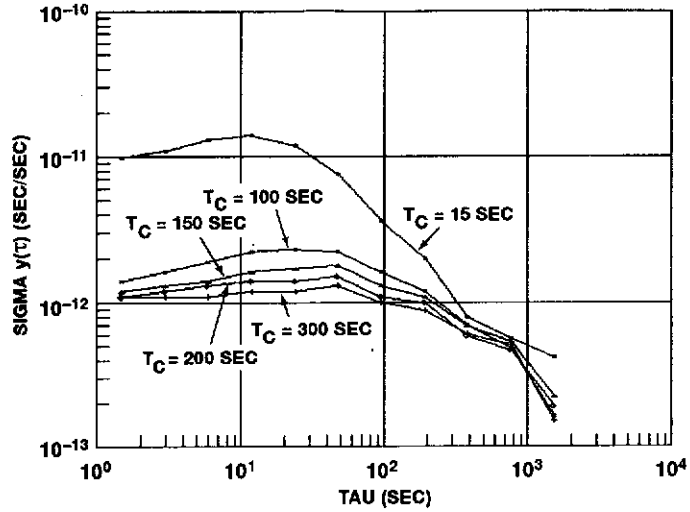


Figure 8: TKS Allan Variance When Using RAFS (Variation With Loop Time Constant)

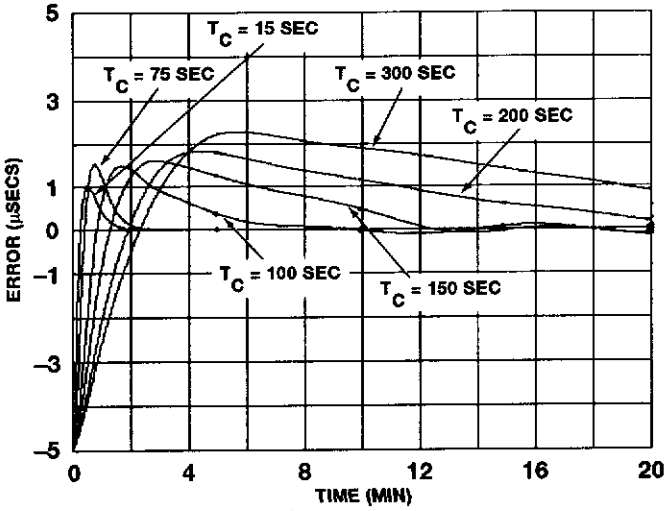


Figure 9: Loop Transient Response When Using RAFS (Variation With Loop Time Constant)

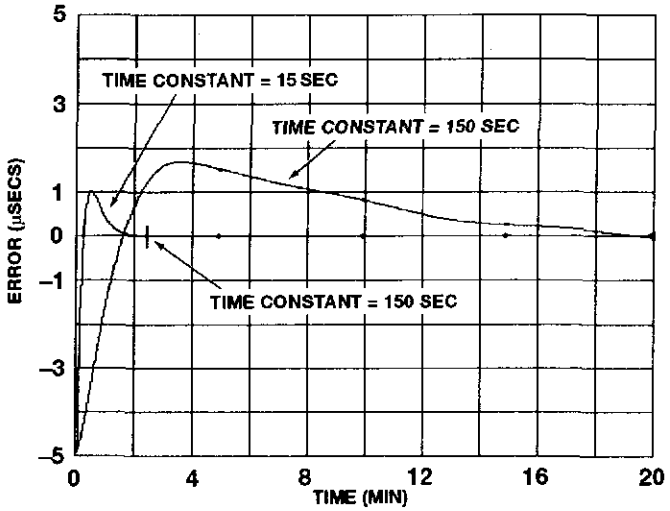


Figure 10: Loop Transient Response When Using RAFS (Single Vs Dual Loop Time Constants)

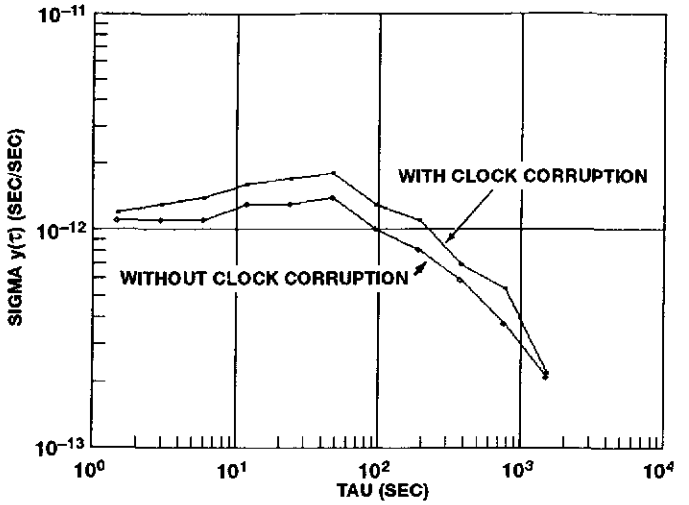


Figure 11: PLL Output Allan Variance When Using RAFS (With And Without Clock Corruptions)

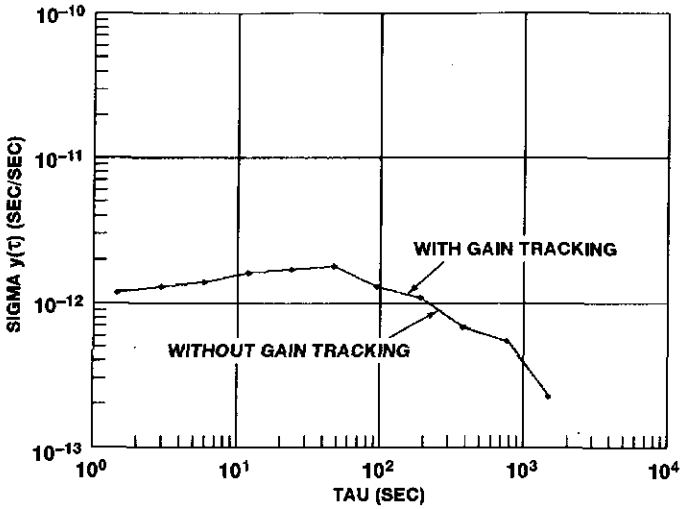
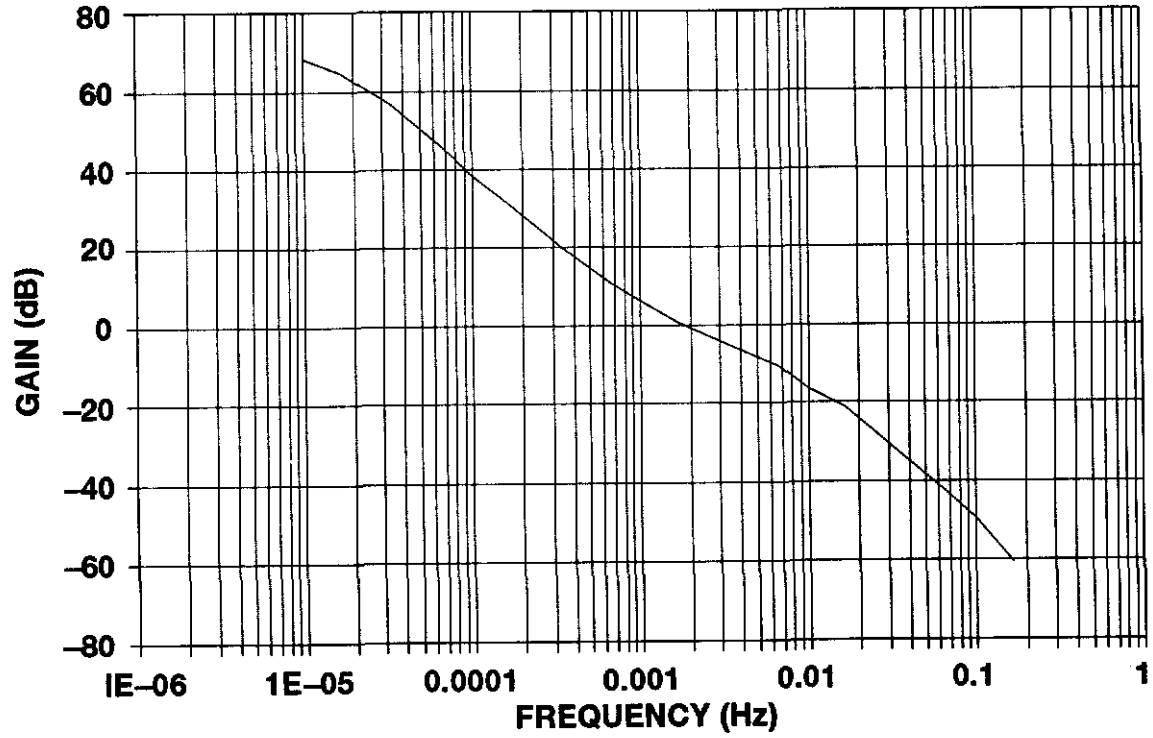
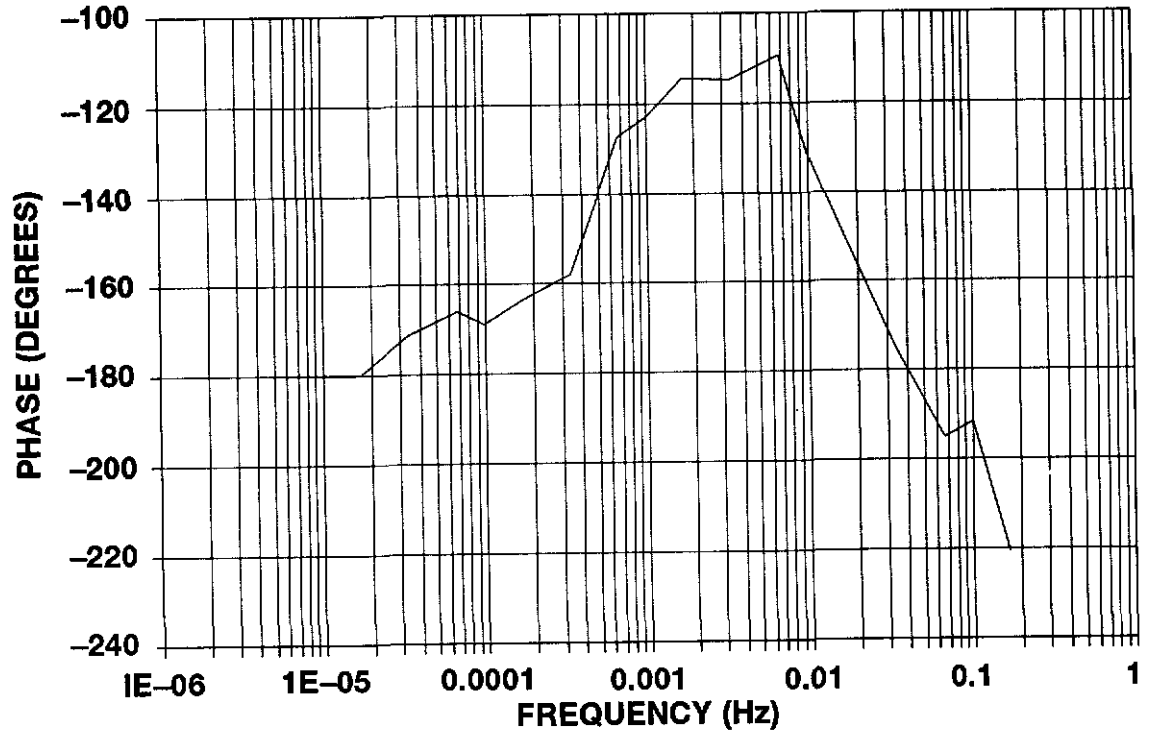


Figure 12: PLL Output Allan Variance When Using RAFS (With And Without Gain Tracking)



(a) Gain Plot



(b) Phase Plot

Figure 13: Bode Plot for the PLL
(With Clock Corruptions and Gain Tracking)